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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/547,167	04/11/2000	Joseph Travis Kennedy	100595.0052US1	4380

7590 07/23/2003

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EXAMINER	
NOVACEK, CHRISTY L	
ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 07/23/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

AA

Office Action Summary	Application No.	Applicant(s)	
	09/547,167	KENNEDY ET AL.	
	Examiner	Art Unit	
	Christy L. Novacek	2822	

-- The MAILING DATE of this communication appears on the cover sh et with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 May 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6,8-15,17-27 and 29-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,8-15,17-27 and 29-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

This Office Action is in response to the amendment filed May 16, 2003.

Response to Amendment

The amendment of claims 5, 8, 12, 13, 16, 26, 29 and 33 is sufficient to overcome the objections to claims 5, 8, 12, 13, 16, 26, 29 and 33 stated in the previous Office Action. Therefore, these objections are withdrawn.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 8-12 and 29-33 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. As amended, claims 8 and 29 recite the limitations of forming "an etchstop layer" on the intermetal organic dielectric layer, a second organic intermetal dielectric layer on the etchstop layer and "a second hardmask layer" on the second intermetal dielectric layer. The specification does not provide support for forming a first hardmask layer, an etchstop layer AND a second hardmask layer.

Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claims 1-6, 8-15 and 17-27 and 29-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art in view of Hussein et al. (US 6,037,255, previously cited), Avanzino et al. (US 5,795,823, previously cited) and Pellerin et al. (US 6,228,758, previously cited).

In reference to claims 1, 12 and 33, the admitted prior art discloses depositing a stack comprising a first organic intermetal dielectric layer (102) and a hardmask layer (103) onto a substrate (100). A via opening (104) is formed in the stack and a sacrificial dielectric (105) is deposited into the opening, such that the opening is substantially filled and the top surface of the stack is substantially covered. A photoresist material (106) is deposited on the sacrificial dielectric. The photoresist is developed and a line opening (107) aligned with the via opening is formed in the stack and inorganic dielectric and the line and via openings are filled with conducting material (Fig. 1a-1d; pg. 3, ln. 7-pg. 4, ln. 12). The admitted prior art discloses using an organic material to comprise the sacrificial layer but also discloses that by using organic material to comprise sacrificial layer, this process typically results in degradation of the critical dimensions of the interconnect pattern (pg. 3, ln. 25-29). Like the admitted prior art, Avanzino ('823) also discloses a process of using a sacrificial layer to etch a line/via interconnect pattern. However, Avanzino teaches that it is advantageous to use a sacrificial layer which can be etched selectively to the intermetal dielectric in order to improve the accuracy of the etch, and thus improve the definition of the interconnect structure (col. 2, ln. 2-5; col. 5, ln. 4-16). Avanzino discloses that the intermetal dielectric (52) may be organic and also discloses that the sacrificial dielectric (70) may be inorganic. Like the admitted prior art and Avanzino, Pellerin also

discloses a process of using a sacrificial layer (24) to etch a line/via interconnect pattern. And like Avanzino, Pellerin also discloses that it is advantageous to use a sacrificial layer which can be etched selectively to the intermetal dielectric (16) (Fig. 1-5; Abstract; col. 4, ln. 65-col. 5, ln. 1). Specifically, Pellerin recommends that when using an organic intermetal dielectric layer, the sacrificial dielectric should comprise an inorganic, silicon based material (col. 4, ln. 65-col. 5, ln. 1). At the time of the invention, it would have been obvious to one of ordinary skill in the art to replace the sacrificial layer of the admitted prior art with a material that has a high etching selectively with respect to the intermetal organic dielectric layer as is taught by Avanzino. Furthermore, in light of the teachings of Pellerin, it would have been obvious to one of ordinary skill in the art to form the sacrificial dielectric layer from an inorganic material in order to provide the high degree of etching selectivity required for precise definition of the interconnect structure.

Regarding the hardmask layer, the admitted prior art discloses it to be "inorganic" but does not specifically state from what material it is made (pg. 3, ln. 9). Like the admitted prior art, Hussein discloses a method of forming conductive interconnections in an organic dielectric layer, wherein a hardmask layer is deposited on the surface of the organic dielectric layer to enhance etching the interconnection opening into the dielectric layer (col. 3, ln. 18-47). Hussein discloses that the hardmask layer preferably comprises silicon oxide (col. 3, ln. 39-41; col. 4, ln. 66-col. 5, ln. 2). At the time of the invention, it would have been obvious to one of ordinary skill in the art to compose the "inorganic" hardmask layer of the admitted prior art of silicon oxide because Hussein teaches that silicon oxide can be used successfully with organic dielectric layers such as that of the admitted prior art.

In reference to claims 2, 3, 23 and 24, Avanzino discloses that a number of insulating materials may be used in accordance with his invention (col. 8, ln. 39-45). Pellerin specifically discloses that the sacrificial inorganic dielectric layer may be made of a silicate, a silsesquioxane, a silica gel, or methyl silsesquioxane (col. 4, ln. 10-15; col. 4, ln. 61-col. 5, ln. 1). These compounds would inherently have the ratio of H, Si, O and R that are stated in claim 2 of the present application. At the time of the invention, it would have been obvious to one of ordinary skill in the art to use one of the inorganic materials such as the methyl siloxane disclosed by Pellerin to comprise the sacrificial dielectric because Avanzino discloses that any number of insulating materials that are known in the art may be used to comprise the sacrificial layer.

In reference to claims 4 and 25, the admitted prior art does not disclose what material the organic intermetal dielectric is made from. Avanzino discloses that organic intermetal dielectrics comprising polyimides are known in the art (col. 8, ln. 51-53). Pellerin discloses comprising the organic intermetal dielectric layer of a material such as a poly arylene ether, an oligomeric hydrocarbon, a poly(paraxylylene), a poly(tetrafluoroethylene), a polyimide, or a divinyl siloxane (col. 4, ln. 2-11).

In reference to claims 5 and 26, the admitted prior art discloses forming a diffusion barrier layer (101) between the substrate (100) and the organic intermetal dielectric layer (102) (pg. 3, ln. 7-9).

In reference to claims 6, 9, 14, 27, and 30, the admitted prior art discloses that a diffusion barrier layer typically comprises silicon nitride (pg. 6, ln. 26-27).

In reference to claims 8 and 29, the admitted prior art discloses forming a diffusion barrier layer (101) between the substrate (100) and the organic intermetal dielectric layer (102) and also forming a hardmask layer (103) on the organic intermetal layer (pg. 3, ln. 7-9).

Avanzino discloses that, as an alternative to forming one organic intermetal dielectric layer, two organic intermetal dielectric layers may be used with the two layers being separated by an etch stop layer in order to more precisely etch separate line and via portions (col. 6, ln. 12-20). At the time of the invention, it would have been obvious to one of ordinary skill in the art to substitute two organic layers with an etch stop layer in between as taught by Avanzino for the single organic layer disclosed by the admitted prior art, in order to obtain more precise etching of the separate line and via portions.

In reference to claims 10 and 31, the admitted prior art discloses that etch stop layers typically comprise silicon oxide (pg. 7, ln. 13-14).

In reference to claims 11 and 32, Avanzino discloses using organic intermetal dielectric layers such as polyimide and also discloses that both the first and second intermetal dielectric layers may be made of the same material (col. 8, ln. 51-52; col. 6, ln. 1-28). PTFE, parylenes, fluorinated and non fluorinated poly(arylene ethers), polymeric material obtained from phenyl-ethynylated aromatic monomers, and fluorinated amorphous carbon are all well-known in the art for the purpose of forming interlevel dielectric layers. At the time of the invention, it would have been obvious to one of ordinary skill in the art to form the organic dielectric layer of Avanzino using any art-recognized equivalent organic dielectric layer.

In reference to claim 13, the admitted prior art discloses using only one organic intermetal dielectric layer. Avanzino discloses that, as an alternative to using only one intermetal dielectric layer, two intermetal layers may be used. The bottom intermetal layer (52a") is made of a material that is different than the second intermetal layer (52b") so that the etching selectivity of the two layers with respect to each other can be used to precisely etch separate line and via portions (Fig. 4a"; col. 6, ln. 20-28). Avanzino discloses that intermetal dielectric layers

may be made of either organic or inorganic materials, but does not specifically disclose using a bottom inorganic layer with an overlying organic layer. Avanzino discloses that any number of insulating materials that are known in the art may be substituted for the materials specifically disclosed in their patent (col. 8, ln. 39-45). Pellerin discloses that when forming a line/via interconnect structure, it is advantageous to use two different intermetal layers. The bottom intermetal layer (16) is used to form the via portion of the interconnect and may be made of an inorganic material. The top intermetal layer (24) is used to form the line portion of the interconnect and may be made of an organic material (col. 4, ln. 61-col. 5, ln. 1). The two intermetal layers of different etching selectivities provide precise etching of the separate line and via portions. At the time of the invention, it would have been obvious to one of ordinary skill in the art to replace the single intermetal layer of the admitted prior art with two intermetal layers that have a high etching selectively with respect to each other (such that the bottom layer may comprise an inorganic material while the top layer comprises an organic layer) in order to provide the high degree of etching selectivity required for precise definition of the separate line and via portions of each interconnect structure.

In reference to claim 15, Avanzino discloses that a number of insulating materials may be used in accordance with his invention (col. 8, ln. 39-45). Pellerin specifically discloses that the inorganic intermetal dielectric layer may be made of a silicate, a silsesquioxane, a silica gel, or methyl silsesquioxane (col. 4, ln. 10-15; col. 4, ln. 61-col. 5, ln. 1). These compounds would inherently have the ratio of H, Si, O and R that are stated in claim 2 of the present application. At the time of the invention, it would have been obvious to one of ordinary skill in the art to use one of the inorganic materials disclosed by Pellerin to comprise the bottom layer of the

intermetal dielectric because Avanzino discloses that any number of insulating materials that are known in the art may be used to comprise the insulating layers.

In reference to claims 17 and 34, the Pellerin discloses that the type etchant used to etch the sacrificial inorganic layer is a matter of design choice that will depend upon the materials selected for the both the first intermetal layer and the sacrificial (col. 5, ln. 21-32). The admitted prior art discloses that a buffered oxide etch can be conducted using *standard* mixture of HF and H_2O. At the time of the invention, it would have been obvious to one of ordinary skill in the art to choose an appropriate etchant such as a buffered oxide etch, as a matter of design choice, based upon the specific type of dielectric layers being utilized.

In reference to claims 18 and 35, the admitted prior art does not disclose what the conducting material is comprised of. Avanzino and Pellerin discloses that the conductive interconnect material may be made of a copper or aluminum alloy or tungsten (col. 1, ln. 30-34 and col. 4, ln. 59-60 of Pellerin; col. 7, ln. 23-40 of Avanzino). At the time of the invention, it would have been obvious to one of ordinary skill in the art to form the conducting layer of the admitted prior art from an aluminum, copper, or tungsten-containing material because, in the absence of the disclosure of any particular conducting material, one of ordinary skill in the art would look to a conventional material with which to form the interconnect metallization.

In reference to claims 19 and 36, the admitted prior art does not disclose forming a conducting diffusion barrier material in conjunction with the conductive material. Pellerin discloses that a conductive liner comprising tantalum or titanium may be used in conjunction with the conductive material to fill in the via/line metallization portions (col. 5, ln. 56-60). Liners of this type are well known in the art to provide a barrier to diffusion of the bulk conducting interconnect material. At the time of the invention, it would have been obvious to

one of ordinary skill in the art to provide a liner to the via/line of the admitted prior art because it is conventional in the art to do so in order to prevent diffusion of the bulk conducting interconnect material into the surrounding insulative layers.

In reference to claims 20 and 37, the admitted prior art does not disclose what the substrate (100) is comprised of. However, Avanzino and Pellerin disclose that typical substrates upon which interconnect metallization layers are built upon include semiconductor wafers, dielectric layers and metal interconnect layers in integrated circuits (col. 8, ln. 45-51 of Avanzino; col. 3, ln. 34-46 of Pellerin). At the time of the invention, it would have been obvious to one of ordinary skill in the art to form the interconnect metallization of the admitted prior art upon a substrate of semiconductor wafers, dielectric layers or metal interconnect layers in integrated circuits because these are all conventional substrates upon which interconnect metallization is formed.

In reference to claims 21 and 38, the admitted prior art discloses forming the via and line openings by etching the hardmask layer with a fluorocarbon based plasma and the organic intermetal dielectric layer is etched with an oxygen based plasma (pg. 3, ln. 30-pg. 4, ln. 4).
In reference to claim 22, the admitted prior art discloses that dual damascene methods may comprise either "via first" methods in which the via openings are etched in a stack of dielectric layers before conducting line openings are etched or "line first" methods in which line openings are etched before via openings are etched. Although the only embodiment described in detail by the admitted prior art is a "via first" dual damascene method, at the time of the invention, it would have been obvious to one of ordinary skill to form the same interconnect structure using an equivalent "line first" dual damascene process as an alternative to the "via first" process

because, as discussed by Applicants' admitted prior art, both damascene processes are well-known equivalent processes.

Response to Arguments

Applicant's arguments filed May 16, 2003 have been fully considered but they are not persuasive.

In response to the rejection of claims 1 and 22 under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art in view of Hussein et al., Avanzino et al. and Pellerin et al., applicant argues that Hussein discloses making the hardmask out of "silicon dioxide" instead of "silicon oxide" as is recited in claims 1 and 22. This argument is not convincing because silicon dioxide is a silicon oxide. Contrary to applicant's assertion that "silicon oxide" refers only to SiO, "silicon oxide" is actually a generic term for any one of a class of SiO_x compounds. Both silicon dioxide (SiO_2) and silicon monoxide (SiO) are silicon oxides. This is supported by the attached articles as well as the attached patent application publication (see paragraph 0034), which demonstrate that "silicon oxide" is conventionally used to describe both silicon dioxide and silicon monoxide. As recited in claims 1 and 22, the term "silicon oxide" has been given its broadest reasonable interpretation. See *In re Zletz*, 893 F.2d 319, 321-22, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989) in which the Court stated, "During patent examination the pending claims must be interpreted as broadly as their terms reasonably allow...". Furthermore, there is no language in applicant's claims or specification that restricts the term "silicon oxide" to refer only to silicon monoxide (SiO).

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christy L. Novacek whose telephone number is (703) 308-5840. The examiner can normally be reached on Monday-Thursday and alternate Fridays 7:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (703) 308-4905. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

AMIR ZARABIAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

CLN
July 17, 2003